### REMARKS

Claims 20-47 are pending in this application. Claims 23, 28, and 41 are proposed to be amended and claim 48 is proposed to be added. These amendments should be entered because they do not add limitations requiring further search or consideration and clarify the issues for appeal.

### 35 U.S.C. §112

Applicant appreciates the indication that this ground of rejection has been withdrawn.

### 35 U.S.C. §102

The Office has rejected claims 20, 22-24, 26-28, 32-34, 38-41, and 45-47 under 35 U.S.C. §102(b) over Higgins (U.S. Patent No. 6,294,405) for the reasons noted on pages 2-6 of the Office Action. Applicant respectfully traverses this rejection.

All of the rejected claims contain a first limitation that a chip pad is formed on or over a substrate and then a RDL pattern is provided on the chip pad. Some of the rejected claims contain a second limitation that there exists no under bump metal under the stud bump. And other of the rejected claims recite a similar limitation that the stud bump is provided on portion of the RDL pattern not covered by the insulating layer without using an under bump metal.

The Office, however, has failed to show that Higgins anticipates such limitations in the claims. The Office cites to Figure 1 of Higgins as anticipating the rejected claims. Figure 1 describes a device containing contact pads 14, redistribution traces 16, under bump metallization (UBM) pads 15, and solder bumps 20. The text accompanying Figure 1 describes that the redistribution traces 16 are "connected to" the contact pads 14. See column 2, lines 41-42. Such a description is consistent with Figure 1 which does not show that the redistribution traces 16 are

located on or over the contact pads 14. Thus, the Office has failed to show that Higgins discloses a feature that anticipates this first claim limitation.

Neither has the Office substantiated that Higgins anticipates the second claim limitation. The Office argues that the UBM pad 15 is not relied on in rejecting the claims and that the rejection uses the redistribution line 16 and the solder bump 20 attached thereto through an opening in the insulating layer 18. In arguing the rejection in this manner, however, the Office ignores the rest of the device as taught in Figure 1.

The device in Figure 1 depicts that solder bumps 20 that are clearly located on UBM pads 15. The text accompanying Figure 1 also describes that the redistribution traces 16 terminate at under bump metallization (UBM) pads 15 and that solder bumps 20 are formed respectively on the UBM pads. See column 1, lines 44-49. Thus, the skilled artisan would have understood from Figure 1 that the solder bumps 20 are formed on UBM pads 15. As well from the text, the skilled artisan would understood that the portions of the redistribution trace 16 under the solder bump 20 are UBM pads, even though not actually depicted in Figure 1. This understanding would be supported by the general knowledge of the skilled artisan since both the solder bumps 20 "in combination with" the UBM pads 15 are "together" generally referred to as electrical contacts. See column 3, lines 2-4.

In rejecting the claims, the Office appears to ignore both of these disclosures. The rejected claims recited that the stud bumps are not formed on a UBM layer. But Figure 1 clearly shows the use of UBM pads and the text accompanying Figure 1 also describes the use of UBM pads.

Thus, the Office has not shown that Higgins teaches or suggests each and every limitation in the rejected claims. Accordingly, Applicant requests withdrawal of this ground of rejection.

6/16/2005 - 7 -

## 35 U.S.C. §103

The Office has rejected claims 21, 25, 29-31, 35-37, and 42-44 under 35 U.S.C. §103 as being unpatentable over Higgins in view of Chakravorty (U.S. Patent No. 6,350,668) for the reasons noted on pages 6-11 of the Office Action. Applicant respectfully traverses this rejection.

As noted above, the rejected claims contain a first limitation that a chip pad is formed on or over a substrate and then a RDL pattern is provided on the chip pad. Some of the rejected claims contain a second limitation that there exists no under bump metal under the stud bump. And other of the rejected claims recite a similar limitation that the stud bump is provided on portion of the RDL pattern not covered by the insulating layer without using an under bump metal.

But the Office has not shown that Higgins teaches or discloses these limitations in the claims as detailed above. And the Office has not argued—much less alleged—that Chakravorty teaches or suggests these limitations. Thus, the Office cannot substantiate that the combined teachings of these references suggest these limitations.

Indeed, it would be difficult for the Office to argue that Chakravorty teaches or suggests these limitations. Figures 3-9 show a semiconductor package containing UBM layer 310. And the semiconductor package illustrated in Figures 10a through 10h does not contain a redistribution layer. See column 13, lines 30-38.

The Office recognizes that Higgins fails to teach a method comprising the step of providing a solder ball on the stud bump. The Office notes that Chakravorty discloses the use of a solder ball 313 on a solder stud 311. The Office concludes that it would have been obvious to substitute the method of Chakravorty for the method disclosed by Higgins because they are known equivalent techniques.

- 8 -

6/16/2005

Applicant disagrees that the method disclosed by Higgins and the method of Chakravorty are equivalents. The method used by Higgins to attach the solder ball 58 to the solder bump 20 is used so that substrate 50 (including all the components) is placed between the solder ball 58 and solder bump 20. Chakravorty merely places the solder ball on the solder bump with nothing in between.

Assuming, *arguendo*, that the methods are equivalent, the skilled artisan would have been motivated to not substitute the method of Chakravorty for the method of Higgins. In making the proposed substitution, the skilled artisan would have modified the device of Higgins to locate the solder balls 58 directly on the solder bumps 20, thereby removing the substrate 50 and all its components. But the substrate 50 and all its components served an important function in the device of Higgins. This reference teaches that using the substrate 50 permits array bonding rather than peripheral bonding, allowing a large size differential between the substrate and the die and allowing shorter bonding leads that are damaged less. *See column 4, lines 18-24*. Thus, by using the substrate 50, the device of Higgins has not only an improved interconnection reliability, but also a decreased footprint. *See column 5, lines 58-62*.

In light of such a disclosure, the skilled artisan would not have been motivated to modify the references as proposed by the Office and remove the substrate 50 of Higgins. Such a modification would have rendered Higgins unsatisfactory for its intended purpose of an improved interconnection reliability and a decreased footprint. See M.P.E.P. § 2143.01.

Thus, the Office has not shown that the combination of the cited references teaches or suggests each and every limitation in the rejected claims. Accordingly, Applicant requests withdrawal of this ground of rejection.

6/16/2005

Serial No. 10/618,113 Attorney Docket No. 11948.0021

# CONCLUSION

For the above reasons, as well as those of record, Applicant respectfully requests the Office to withdraw the above grounds of rejection and allow the pending claims.

If there is any fee due in connection with the filing of this Amendment, including a fee for any extension of time not accounted for above, please charge the fee to our Deposit Account No. 50-0843.

Respectfully Submitted,

KENNETH E. HORTON

Reg. No. 39,481

Date: June 16, 2005

6/16/2005 - 10 -